CLAIMS:

1. An integrated circuit having a microprocessor comprising:

a configurable portion comprising one of a plurality of microcode sets, wherein each of the plurality of microcode sets is associated with a different set of macroinstructions; and

a non-configurable portion comprising sequencing logic that is the same for each one of the plurality of microcode sets.

2. The integrated circuit of claim 1 wherein the microprocessor further comprises a datapath unit configured to execute each different set of macroinstructions.

3. The integrated circuit of claim 2 wherein the datapath unit is coupled to a configurable logic block.

4. The integrated circuit of claim 1 wherein each microcode set of the plurality of microcode sets is associated with a microprocessor of a plurality of microprocessors.

5. The integrated circuit of claim 1 wherein the IC is a field programmable gate array.